

What is claimed is:

1. A system for reducing interference in a communication system, the interference occurring on a data sample signal having a precursor inter-symbol interference (ISI) portion and a post-cursor ISI portion, the system comprising:
  - a first precursor equalizer, for receiving the data sample signal and for performing an equalization operation on said data sample signal to reduce the precursor ISI and to generate an ISI equalized sample signal;
  - a summer, coupled to said first precursor equalizer, for combining said ISI equalized sample signal and a post-cursor cancellation signal to generate an equalized estimated sample signal;
  - a slicer, coupled to said summer to receive said equalized estimated sample signal, for generating a detected symbol signal representing a preliminary symbol value of said equalized estimated sample signal;
  - a precursor canceller, for receiving said equalized estimated sample signal and said detected symbol signal, for further reducing the precursor interference, said precursor canceller having:
    - a finite impulse response filter, for receiving said detected symbol signal and for determining the precursor ISI on said detected symbol signal to generate a precursor cancellation signal,
    - a first delay component to receive said equalized estimated sample signal, for delaying said equalized estimated sample signal by a first amount and to output a delayed equalized estimated sample signal, said first amount corresponding to a delay caused by said slicer and finite impulse response filter,

a DPIC summer to combine said precursor cancellation signal and said delayed equalized estimated sample signal to generate a second output signal representing said data sample signal having a reduced precursor interference portion; and

a first post-cursor canceller, for receiving said detected symbol signal, and for reducing the post-cursor interference on said detected symbol signal to generate said post-cursor cancellation signal.

2. The system of claim 1, wherein said post-cursor canceller includes a plurality of taps having input coefficients.

3. The system of claim 2, wherein said coefficients automatically adjust in response to the post-cursor interference on the data sample signal.

4. The system of claim 1, wherein said first precursor equalizer includes a plurality of taps having input coefficients to reduce the pre-cursor interference.

5. The system of claim 1, wherein said finite response filter includes a plurality of taps having input coefficients to reduce the pre-cursor interference.

6. The system of claim 1, wherein said first delay component aligns said equalized estimated sample signal and said slicer output signal.

7. The system of claim 1, further comprising:

a second delay component, coupled to receive said data sample signal, for delaying said data sample signal by a second amount and for outputting a delayed data sample signal; and

a second precursor equalizer, for receiving said delayed data sample signal and for performing an equalization operation on said delayed data sample signal to reduce precursor interference and to generate a delayed equalized signal;

wherein said DPIC summer receives said delayed precursor equalized output wherein said delayed equalized estimated sample signal represents said data sample signal having a reduced precursor interference portion.

8. The system of claim 7, wherein said second amount corresponds to a delay caused by said first precursor equalizer, said summer, and said first delay component reduced by the delay caused by said second precursor equalizer.

9. The system of claim 7, wherein said second precursor equalizer includes a plurality of taps having input coefficients to reduce the pre-cursor interference.

10. The system of claim 7, further comprising:

a DPIC slicer, coupled to said DPIC summer to receive said second output signal, for generating a DPIC slicer output signal representing a preliminary value of said second output signal; and

a second post-cursor canceller, for receiving said DPIC slicer output signal, and for reducing the post-cursor interference of said DPIC slicer output signal to generate a DPIC post-cursor cancellation signal;  
wherein said DPIC summer combines said DPIC post-cursor cancellation signal with said precursor cancellation signal, said delayed equalized estimated sample signal and said delayed equalized signal to generate said second output.

11. The system of claim 10, wherein said second post-cursor canceller includes a plurality of taps having input coefficients.

12. The system of claim 11, wherein said coefficients automatically adjust in response to the post-cursor interference on the data sample signal.